Mitigation of Common mode Noise for PFC Boost Converter by Balancing Technique

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Abstract

The PFC Boost Converter is an integral part of modern power supplies to improve power factor in electronic devices. The inherent problem associated with it is common mode (CM) Electromagnetic interference (EMI) noise arising due to the higher switching transition rate (dv/dt). The main coupling path for the CM noise is provided by parasitic capacitance occurring between the switching node and ground. In this scenario, it is important to identify feasible solutions for CM noise reduction. This paper therefore develops a circuit model for a boost PFC converter allowing detailed analyses of the performance of this type of converter. It includes all parasitic components along the CM noise path. Using this CM noise model, a novel balancing approach is proposed that mitigates CM noise in a PFC boost converter. Validation of the new design approach is supported by experimental results demonstrating substantial noise reduction for a balanced PFC boost converter.

1 Introduction

The subject of a reliable and efficient regulated power supply has attracted significant attention in recent years due to technological advancements in electronics. Mostly, switch mode power supplies (SMPS) are used in modern systems due to subsequent advantageous over linear power supplies such as higher power performance, reliability and cost [1]. However, higher switching frequencies are needed in SMPS to reduce the size of components in a converter. These higher switching frequencies often introduce unwanted effects such as Electromagnetic interference (EMI) noise [2]. Moreover, it deteriorates the performance of a converter itself and may affect other electrical equipment attached to the main power source. Additionally, regulatory bodies impose some limitations on EMI emission to regulate safety standards of EMI emission for electrical and electronic products. It is therefore imperative to control EMI to satisfy the requirement of EMC standards.

The conducted EMI noise in converters is generally sub-divided into CM (common mode) and DM (differential mode) noise. Each type has different mechanism of generation and differing propagation paths. CM noise arising from parasitic capacitance flows to ground returning back to both power lines (live and neutral phases). Differential Mode noise is a result of MOSFET switching transitions producing noise that flows through the neutral line, returning back to the phase line. Several techniques have been proposed in the literature to mitigate EMI noise in converters [3-5]. These schemes typically focus on cancellation of noise at its source and or along its propagation path. In the latter case an external EMI filter either passive, active or hybrid is used [6]. Usually, an EMI filter is incorporated inside a converter to mitigate EMI noise. However, there is a practical size limit to the line filtering y-capacitance in an EMI filter which restricts the filtering performance. In contrast, noise reduction at source relies on compensation network techniques such as noise source balance, noise source quasi-balance and active compensation. In the first of these methods, compensation can be performed by existing noise sources of same amplitude and out of phase. In quasi-balance method, the noise sources are balanced by decreasing or increasing the amplitude of noises. In the last technique, an extra circuitry is needed to introduce anti-noise source in a circuit that has equal magnitude and out of phase to original noise present in a circuit.

Our proposed compensation technique is based on the standard reduction of CM noise coupled through the parasitic capacitance of the switching MOSFET [7]. Other researchers have suggested that the balanced switching converter is the best approach for CM noise reduction in a range of different converter topologies [8]. However, the new technique also compensates for the parasitic capacitance of the output diode offering further improvement in noise performance. The technique is applied to a PFC boost converter and compared to the results obtained from unbalanced converter.

2 CM noise model of a converter

Boost PFC converters are normally used to improve power factor correction and it is important to understand the noise generation mechanism for this topology in order to develop noise compensation approaches. The equivalent circuit for a typical boost PFC converter including a Line Impedance Stabilisation Network (LISN) is shown in fig 1. The LISN

stabilizes input impedance for measurement of conducted EMI noise.

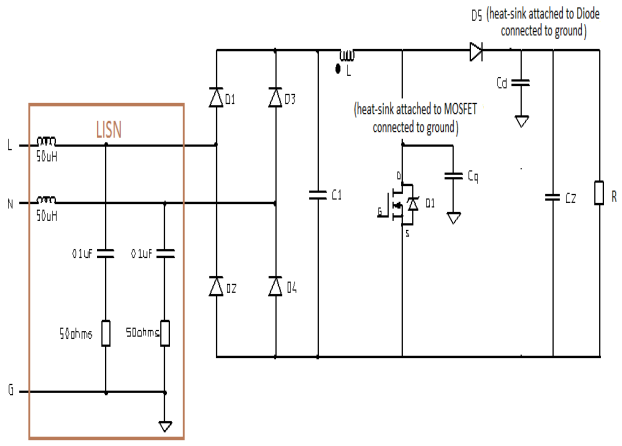

Fig. 1. Off-line PFC Boost converter showing LISN

Figure 2 shows the high frequency components within a boost converter that control voltage and current and includes the associated parasitic elements. In a CM noise model of a boost converter, LISN inductors and capacitors are ignored and the stabilisation network is represented by resistors of 50 Ohm denoted here by R1 and R2. Moreover, for simplicity of the model, the full-bridge diodes are replaced with a short circuit. However, the high frequency inductor model is indicated with EPC (equivalent parallel capacitance) and EPR (equivalent parallel resistance). EPC denotes the winding capacitance occurring within a boost inductor and EPR represents the winding losses of an inductor. The input and output capacitors are included ESR (equivalent series resistance) and ESL (equivalent series inductance). ESR and ESL indicate the existence of resistance and inductance in capacitor plates and leads. The output diode includes the junction capacitance parallel to the diode represented by Cj. The nodes Q and D represent the parasitic capacitance of the switching MOSFET and diode respectively. The development of this model reflects best practice as reported in various published research articles that investigated the effect of parasitic components on EMI noise [9].

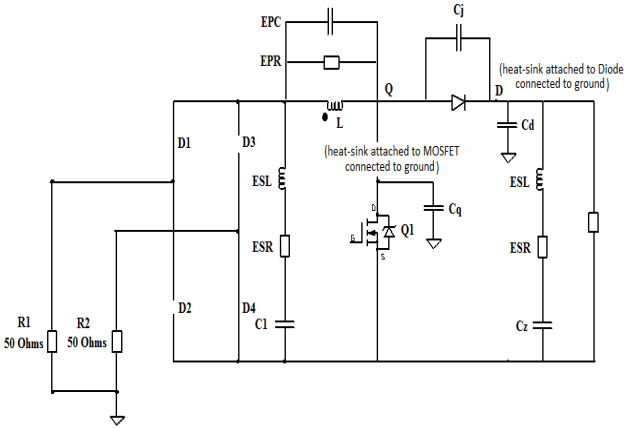

Fig. 2. Off-line PFC Boost converter with its parsitic components

2.1 CM noise generation and coupling path

In most convertors heat sinks are attached to switching devices to provide protection from thermal runway. These heat sinks are usually earthed for safety and this necessitates the introduction of an insulating material between the MOSFET case and heatsink. Consequently this introduces an additional small parasitic capacitance between these two elements. Although the total parasitic capacitance in a convertor is in the pico-farad range the high voltage switching rate will cause substantial current flow through these capacitances resulting in substantial CM noise. It is necessary therefore to consider each of the various parasitic components and introduce techniques to reduce their individual contribution to the CM noise.

The parasitic capacitance between MOSFET drain and ground is denoted with Cq, while the parasitic capacitance between diode cathode and ground is represented with Cd.

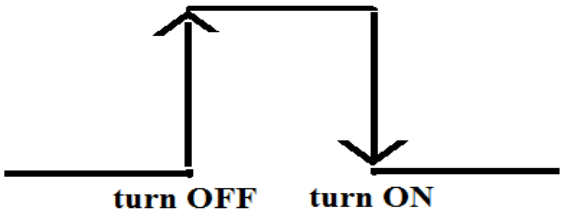

Fig. 3. Voltage transition at node Q due to switching action of MOSFET

In fig. 3, during switching transition from ON to OFF state, the potential at node Q changes from low to high. As a result, the parasitic capacitance is charging due to current flowing through it. During MOSFET turn-on the voltage at point Q falls to zero and D5 becomes reverse biased. The parasitic capacitance of MOSFET Cq discharges through D1 and D4 to LISN resistors R1 and R2 respectively. However, the parasitic capacitance of the output diode Cd also follows the same path by passing through the load capacitor. Thus the CM noise propagation path during MOSFET turn ON is shown in fig 4.

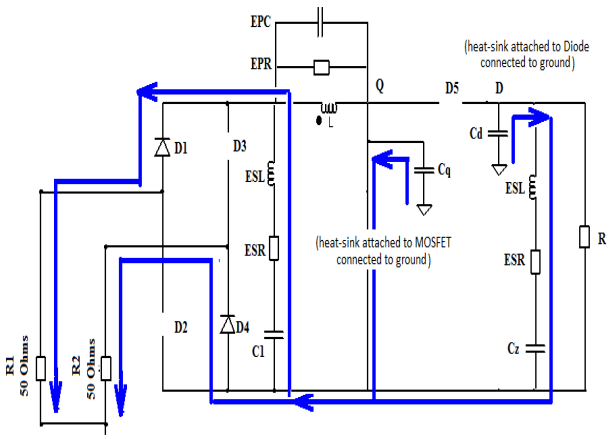

Fig. 4. CM noise coupling path during MOSFET turn ON

Using a similar analysis the CM noise propagation path during the MOSFET turn-off state is as shown in fig 5. The voltage at point Q increases to Vo and D5 conducts. Therefore, the parasitic capacitance of MOSFET Cq charges and CM noise flows to ground returning through LISN resistors R1 and R2. However, the parasitic capacitance of diode Cd also charges up which allowing CM noise to flow to ground and return back through LISN.

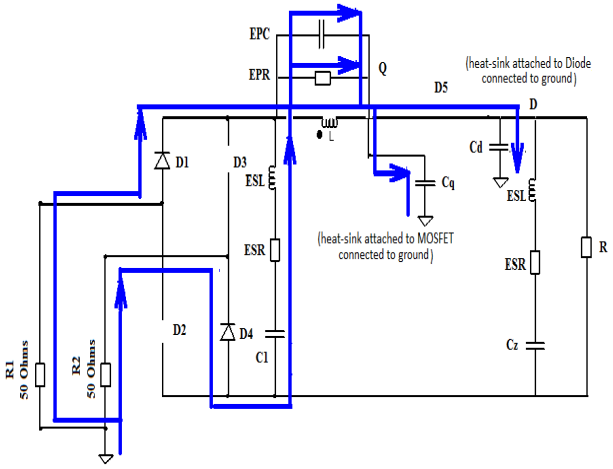

Fig. 5. CM noise coupling path during MOSFET turn OFF

3 Proposed balance technique

The improved technique introduces the antiphase noise source by adding a coupled inductor with compensating winding Nc and compensating capacitor Cq' to generate a complimentary voltage at node Q' as shown in fig 6. The voltage at Q' is 180° out of phase as compared to the voltage at Q producing a current in the opposite direction to cancel out the noise current of Cq. As previously mentioned in a conventional boost converter, the heat-sink of the rectification diode is grounded. However, an additional improvement included in the proposed converter is to attach the heat-sink of rectification diode to the neutral line as shown in fig 6.

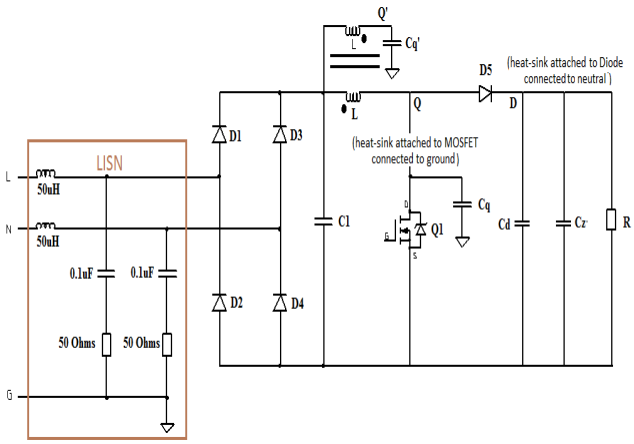

Fig. 6. Off-line proposed balance PFC Boost converter

A parasitic model of the high frequency components of the new balanced PFC boost converter is shown in fig 7. This has similar simplifications to the standard model as previously discussed. The EPC (equivalent parallel capacitance) and EPR (equivalent parallel resistance) are included in the high frequency model of a coupled inductor. Also, the input and output capacitors are included ESR (equivalent series resistance) and ESL (equivalent series inductance). The output diode includes the junction capacitance parallel to diode represented with Cj. The nodes Q and Q' represent the parasitic capacitance of MOSFET and compensation capacitor Cq' respectively.

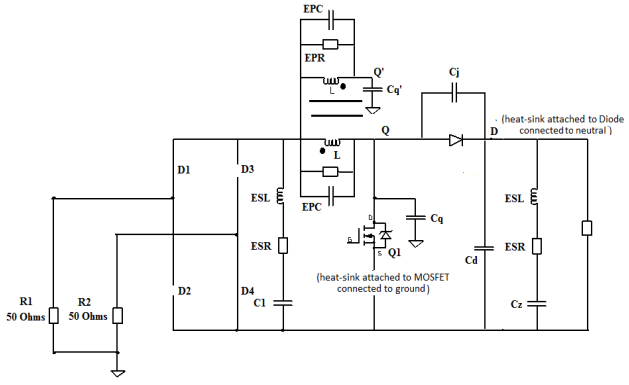

Fig. 7. Off-line proposed balance PFC Boost converter with its parsitic components

During MOSFET turn-on the voltage at point Q falls to zero and D5 becomes reverse biased. The voltage at point Q' is in anti-phase compared to the voltage at Q cancelling the noise produced at point Q. Furthermore, Cd is not contributing to CM noise because it is connected to the neutral line. The CM noise flow path is shown in fig 8.

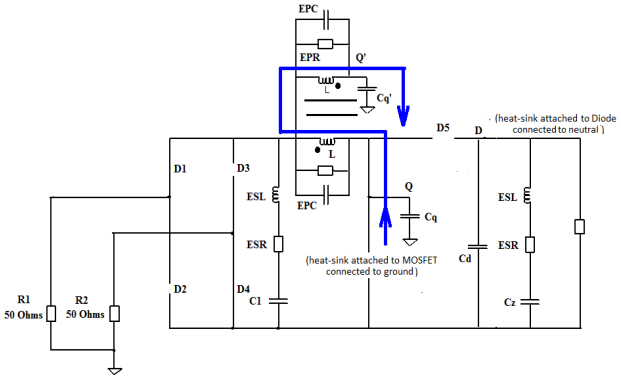

Fig. 8. CM noise coupling path during MOSFET turn ON

During MOSFET turn-off the CM noise propagation path for balanced PFC boost converter is as shown in fig 9. The voltage at point Q rises to reach Vo and D5 conducts. Therefore, the parasitic capacitance of MOSFET Cq charges and CM noise current flows to ground and returns through compensating capacitance Cq'. However, the parasitic capacitance of diode Cd is not contributing to CM noise flow as it is attached to the neutral line.

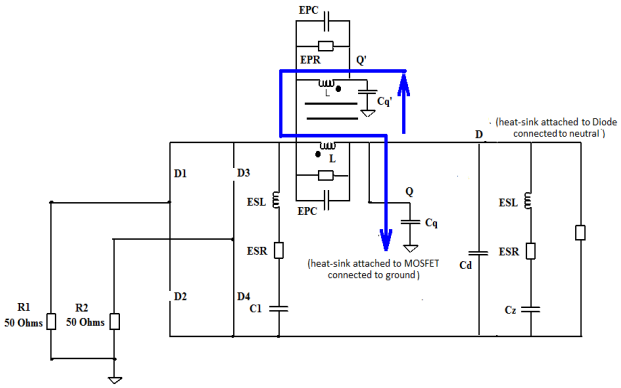

Fig. 9. CM noise coupling path during MOSFET turn OFF

4 Experimental results and discussion

A PFC boost converter with a switching frequency of 125kHz was fabricated and tested in the lab to validate the proposed methodology. The input and output specification of this converter are shown in Table 1 below :

TABLE I.

	Specification	*Value*
1.	Input Voltage	230V
2.	Input frequency	50Hz
3.	Output Voltage	385V
4.	Output Current	0.78A
5.	Output power	300W

Table 1 Specification of test converter

In fig 10, the conducted EMI noise measurements of a typical conventional PFC boost converter are shown. The heat-sinks of the switching MOSFET and output diode are attached to ground in the conventional method. In contrast, the conducted EMI noise measurements of the developed balanced boost converter are shown in fig 11. It is evident from that the peak of EMI noise is at 83dBuV for the conventional approach and reduced to 69dBuV for the balanced boost converter implementation. Therefore, the EMI noise is improved by almost 14dB by using the balancing technique in the boost converter.

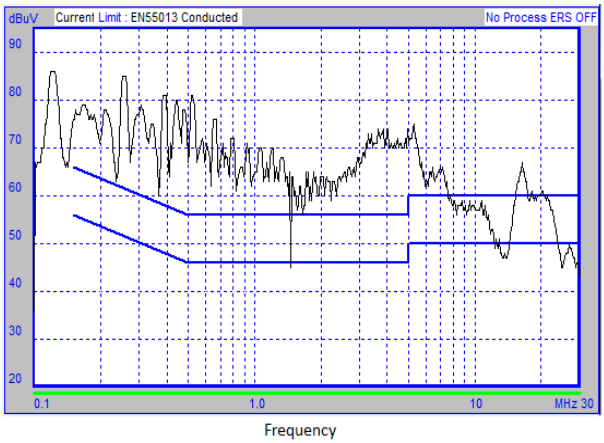

Fig. 10. Conducted EMI noise measurement of conventional PFC boost converter.

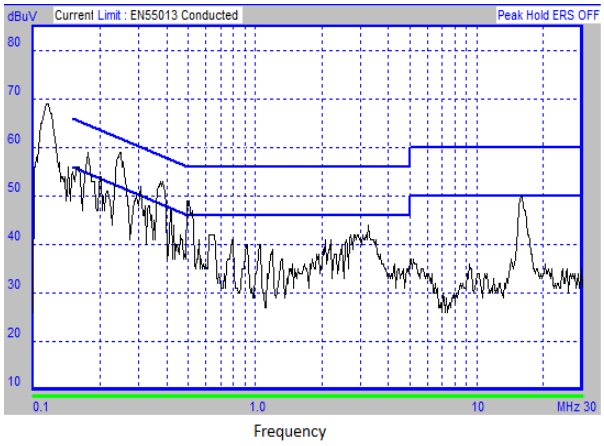

Fig. 11. Conducted EMI noise measurement of balanced PFC boost converter

Conclusion

In this paper, an improved balancing technique was proposed to reduce the overall CM noise of PFC boost converter. Simulation and bench measurements demonstrate that this technique mitigates the CM noise effectively through parasitic capacitance of MOSFET/Diode. It is also confirmed experimentally that the proposed method reduces the noise by nearly 14 dB for the case of a PFC boost converter when compared to the conventional technique. We intend to further

refine the technique and investigate its application in a range of converter topologies.

References

[1] Maniktala, S., 2012. Switching Power Supplies A - Z. Oxford: Newnes

[2] Paul, C.R., 2006. Introduction to Electromagnetic compatibility. Hoboken, New Jersey: John Wiley & Sons

[3] Yang, Y., Huang, D., Lee, F.C. and Li, Q., 2013. Transformer Shielding Technique for Common Mode Noise Reduction in Isolated Converters. Energy Conversion Congress and Exposition. 15-19 Sept. 2013 Denver, CO. IEEE, 4149 – 4153

[4] Kang, B.G., Chung, S., Won, J. and Kim, H., 2015. EMI reduction technique of flyback converter based on capacitance model of transformer with wire shield. 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia). 1-5 June 2015. 163-169

[5] Majid, A., Saleem, J. and Bertilsson, K., 2012. EMI Filter Design for High Frequency Power Converters. International Conference on Environment and Electrical Engineering (EEEIC). 18-25 May 2012 Venice. IEEE, 586 - 589

[6] Biela, J., Wirthmueller, A., Waespe, R., Heldwein, M. L., Raggl, K. and Kolar, J. W., 2009. Passive and active hybrid integrated EMI filters. IEEE Transaction on Power Electronics, 24(5), 1340–1349

[7] S. Lin, M. Zhou, W. Chen and J. Ying, "Novel methods to reduce common-mode noise based on noise balance," in Proc. 2006 IEEE Power Electronics Specialist Conf., pp. 2728 – 2733

[8] Kong, P. and Lee, F.C., 2010. Transformer structure and its effects on common mode EMI noise in isolated power converters. Applied Power Electronics Conference and Exposition. 21-25 Feb. 2010 Palm Springs, CA. IEEE, 1424 – 1429

[9] Neugebauer, T. C. and Perreault, D. J., 2006. Parasitic capacitance cancellation in filter inductors. IEEE Transactions on Power Electronics, 21(1), 282–288