# CM Noise Reduction of Isolated Converter by Balancing Technique

Nasir
Faculty of Science and Technology
Bournemouth University, UK
Bournemouth, UK
nasir@bournemouth.ac.uk

Jon Cobb
Faculty of Science and Technology
Bournemouth University, UK
Bournemouth, UK
jcobb@bournemouth.ac.uk

*Abstract*— **Common mode (CM) Electromagnetic interference (EMI) noise in an isolated converter is mainly due to parasitic capacitance occurring within the SMPS (Switch-mode Power Supply). It flows through transformer coupling capacitance and the parasitic capacitance of MOSFETs and diodes. Several techniques have been proposed in the literature to mitigate the common mode noise flowing through transformer windings. Transformer shielding is one of the most effective methods to reduce EMI noise between the primary and secondary windings, however. However, further improvement should be possible by developing more precise models. In this paper, we develop an EMI noise model for an isolated converter that allows detailed performance analysis. It incorporates the parasitic elements of the converter components and also the coupling capacitance of the transformer. Using this model we propose a new balancing technique to mitigate the CM noise of the isolated converter with modified transformer. The proposed method is applied to an isolated converter and experimental results are provided to verify the novel balancing technique.**

## I. Introduction

Electromagnetic interference (EMI) is defined as an electromagnetic disturbance that limits the performance of electronic and electrical equipment [1]. Therefore, EMI safety standards have been established to guarantee the performance of equipment without degradation.

EMI standards are necessary to meet according to EMC regulatory bodies and EMI filters are designed to mitigate EMI noise to meet these standards. However, there is a practical limit to the line filtering y-capacitance in EMI filter which limits the filtering performance. Conducted EMI noise is categorized into common mode interference (CM) and differential mode interference (DM) noise. The generation and coupling mechanisms are different for each type of interference. The common mode interference is typically caused by parasitic couplings (such as inductive and capacitive) occurring within the SMPS and flows through the ground wire and returns back via the phase and neutral lines. On the other hand, the differential mode interference is mainly due to transistor switching action and flows through the neutral line returning back via the phase line.

To analyze common mode EMI noise, a circuit model is required to identify causes of noise generation and noise propagation paths. In isolated converters, parasitic coupling between primary and secondary windings of the transformer is the main conduction path for CM noise. However, parasitic capacitance between a switch node and ground also provide a path for CM noise.

Several techniques have been proposed in the literature to reduce CM noise [2-6]. The most common techniques to mitigate CM noise are compensation [7], shielding [8,9], and the balancing shielding technique [10]. In the compensation method, a circuit is designed to cancel the effect of noise through parasitic capacitance between the MOSFET drain terminal and ground. In the shielding approach an additional layer between the primary and secondary transformer windings is used to reduce the effect of noise through inter-winding capacitance. In the balancing-shielding technique the combined effect of CM noise produced by parasitic capacitance of MOSFETs and the inter-winding capacitance of transformer windings is reduced along the propagation path.

In this paper, a new balancing technique is proposed to reduce the noise of both parasitic capacitances (such as MOSFET and Diode capacitance) and transformer inter-winding capacitance. Furthermore, the effect of transformer inter-winding capacitance, parasitic capacitance between a switching node and ground will be analyzed in relation to EMI performance. A proposed technique to improve EMI reduction is applied to a flyback based converter and compared to the results obtained from the conventional method.

## II. CM Noise Model of a Converter

Consider a fly-back converter as for example that shown in Fig 1. At the front end of the converter a Line Impedance Stabilization Network (LISN) is normally used to stabilize the impedance to allow measurement of the conducted EMI noise of the converter. In noise measurement, the input and output capacitor acts as a short circuit. The points, Q (across

978-1-5090-0261-0/16/$31.00 ©2016 IEEE

MOSFET) and D (across Diode), in the circuit diagram of Figure 1 indicate the node where dv/dt can introduce switching noise due to the MOSFET and diode.

Cq and Cd represent the parasitic capacitance across the MOSFET and Diode respectively. Cp-s is the inter-winding capacitance between the primary and secondary winding of the transformer. Therefore, the switching action of the MOSFET introduces CM noise at node Q, which can propagate through Cq and Cp-s. Cq and Cp-s act as a parallel capacitance which results in enhancing the overall cm noise. On the other hand, CM noise produced by the Diode can propagate through Cd to ground. Both CM noise from the MOSFET and Diode can propagate to ground.

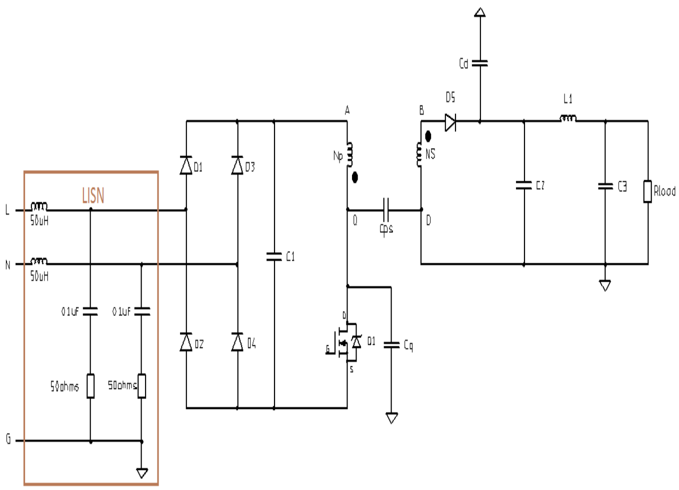


Fig. 1. Off-line fly-back converter showing LISN

## A. Balancing Technique

A new balancing technique for noise reduction is proposed to improve the converter performance. In this scheme, the compensating winding Np-a and compensating capacitor Cq' are added into the circuit to generate complimentary voltage at node Q'. The voltage at Q' is 180° out of phase with the voltage at Q thus producing a current in the opposite direction to cancel out the noise current of Cq. The other advantage of Npa winding is to nullify the effect of noise across Ns by balancing the inter-winding capacitances. Similarly, other compensating winding Nsa and compensating capacitor Cd' are added to neutralize noise current of Cd.

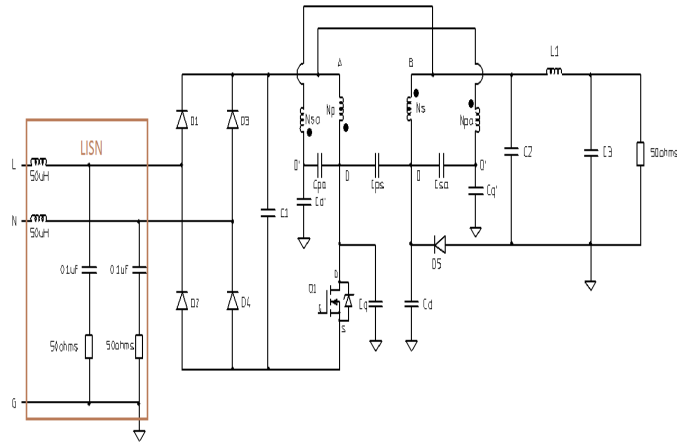


Fig. 2. Off-line fly-back converter with balancing technique

## B. Transformer Winding Construction

The design of the transformer winding for a conventional converter is shown in figure 3. Np and Ns stand for the total number of primary and secondary windings respectively. Cps represents the inter-winding capacitance between primary and secondary coils. On the other hand, the proposed transformer construction is shown in figure 4, which includes Npa and Nsa compensating windings. Npa and Nsa characterize the total number of primary auxiliary and secondary auxiliary windings respectively. Cpa and Csa are the inter-winding capacitances between primary and auxiliary windings and secondary and auxiliary windings respectively.

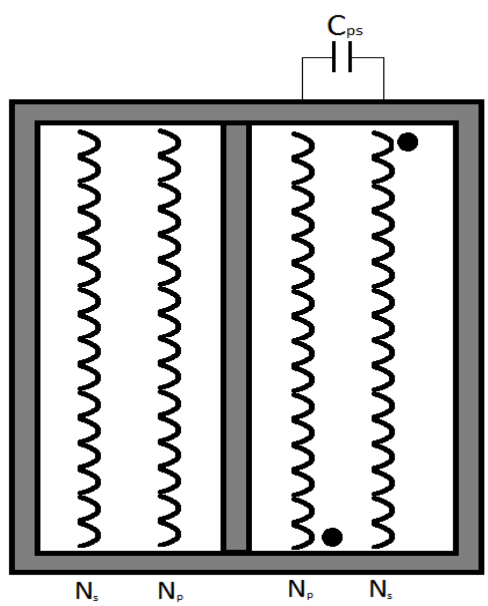


Fig. 3. Conventional Transformer winding construction

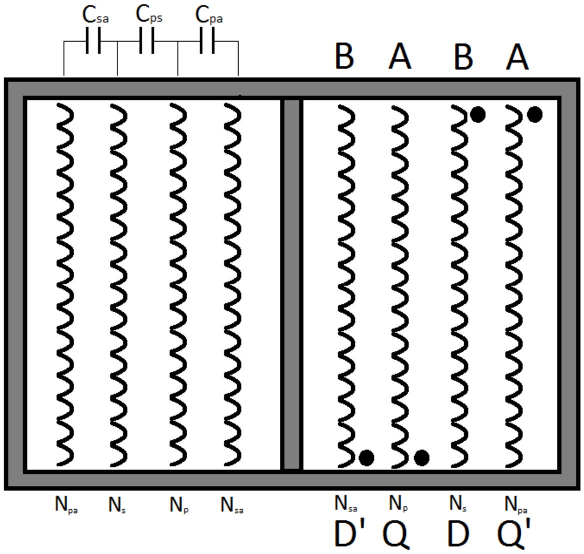


Fig. 4. Transformer winding construction with balancing technique

## *C. Voltage noise distribution across transformer windings*

During MOSFET turn ON

The voltage noise distribution across primary winding, Np, and primary auxilary winding, Npa, are shown in fig 5a. The voltage at nodes Q and Q' are 0V and 2Vin respectively. While the voltage at point A is constant at Vin (input voltage of converter). In fig 5b, the voltage noise distribution across secondary winding Ns is shown and it is clear from the figure that the voltage noise distribution across secondry winding is constant and equal to Vin.

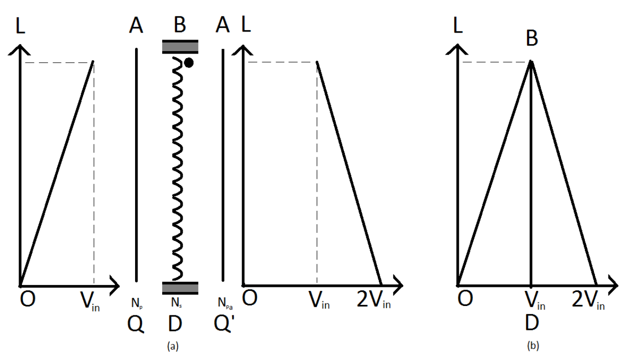


Fig. 5. Voltage noise distribution during MOSFET turn ON (a) across primary and auxilary primary windings. (b) across secondry windings

In fig 6a, the voltage at point D is {Vo + (Vin/N)} and the voltage at point D' is {Vo – (Vin/N)}. While the voltage at point B is constant at Vo (output voltage of converter). In fig 6b, the voltage noise distribution across primary winding Np is shown and it is clear from the figure that the voltage noise distribution across primary winding is constant and equal to Vo.

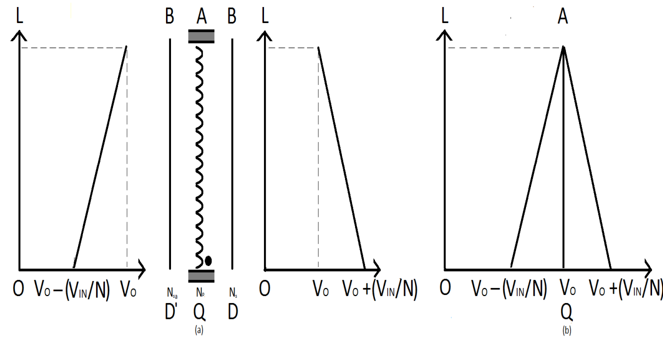


Fig. 6. Voltage noise distribution during MOSFET turn ON (a) across secondary and auxilary secondary windings. (b) across primary windings

During MOSFET turn OFF

The voltage noise distribution across primary winding Np and primary auxilary winding Npa are shown in fig 7a. The voltage at point Q is {Vin + ($V_O$*N)} and the voltage at point Q' is {Vin - ($V_O$*N)}. While the voltage at point A is constant at Vin (input voltage of converter). In fig 7b, the voltage noise distribution across secondary winding Ns is shown and it is clear from this figure that the voltage noise distribution across the secondry winding is constant and equal to Vin.

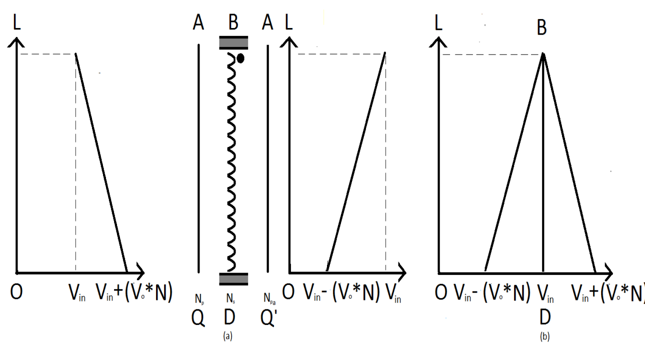


Fig. 7. Voltage noise distribution during MOSFET turn OFF (a) across primary and auxilary primary windings. (b) across secondry windings

In fig 8a, the voltage at point D is 0 and the voltage at point D' is 2Vo. While the voltage at point B is constant at Vo (output voltage of converter). In fig 8b, the voltage noise distribution across primary winding Np is shown and it is evident that the voltage noise distribution across the primary winding is constant and equal to Vo.

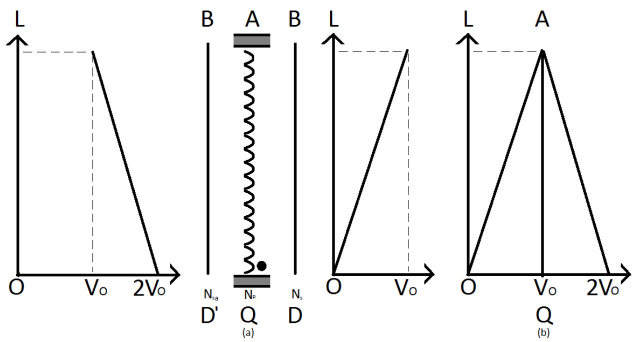


Fig. 8. Voltage noise distribution during MOSFET turn OFF (a) across secondary and auxilary secondary windings. (b) across primary windings

From the above discussion, it is clear that the voltage noise distribution across primary and secondary windings are constant throughout the switching period of the converter. Therefore, the cm noise across both windings should be reduced due to the compensating windings.

## III. EXPERIMENTAL RESULTS AND DISCUSSION

To validate the proposed novel balancing technique, a flyback converter of 132 kHz switching frequency was built and tested. The input and output specifications of this converter are shown in table 1 below

TABLE I.

| | *Specification* | *Value* |
|---|---|---|
| 1. | Input Voltage | 230V |
| 2. | Input frequency | 50Hz |
| 3. | Output Voltage | 12V |
| 4. | Output Current | 1A |
| 5. | Output power | 12W |

Table 1 Specification of test converter.

The results of the Flyback converter using the conventional transformer winding and the corresponding conducted EMI noise measurement are shown in Fig. 9. The results of the new modified balanced transformer winding structure applied to the flyback converter are shown in Fig. 10. The results show that the conducted EMI noise for balanced transformer winding is improved by almost 10 dB.

The proposed technique used the extra windings in a transformer which not only reduce the EMI filter size but also improve the performface of power supply. This would provide the benefits of improved EMI reduction in practical designs compatible with EMI specifications.

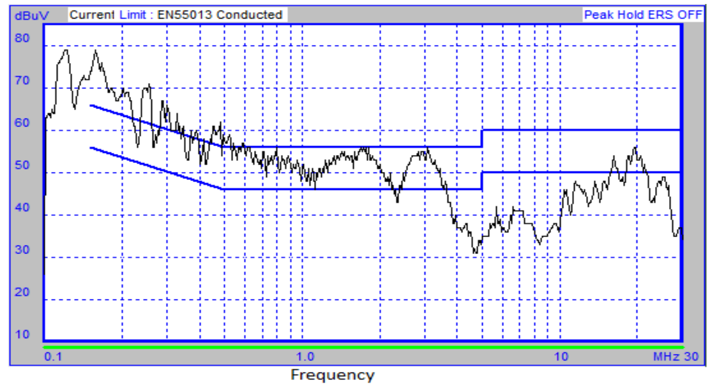


Fig. 9. Conducted EMI noise measurement of power supply with conventional transformer

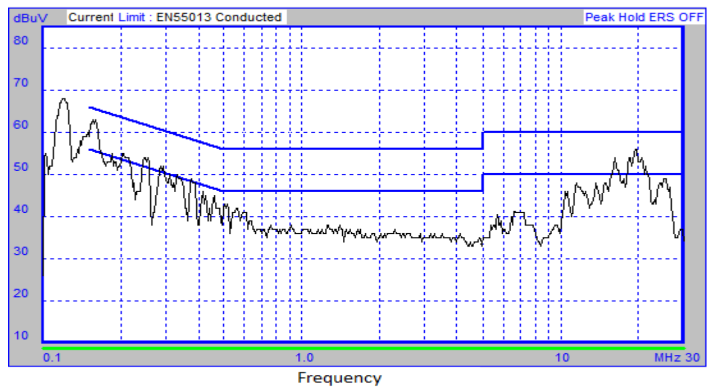


Fig. 10. Conducted EMI noise measurement of power supply with balance transformer

## CONCLUSION

In this paper, a new balancing technique is proposed to reduce the overall cm noise of an isolated converter. This technique mitigates the cm noise not only through parasitic capacitance of MOSFET/Diode but also through inter-winding capacitance by balancing the transformer winding. It is confirmed experimentally that the proposed method works efficiently to overcome the problem of EMI noise in isolated converters and reduces the noise by nearly 10 dB for the case of a flyback converter when compared to conventional technique. We intend to further refine the technique and investigate its application in a range of converter topologies.

## REFERENCES


[1] Paul, C.R., Introduction to Electromagnetic compatibility. Hoboken, New Jersey: John Wiley & Sons, 2006

[2] P. Kong , S. Wang, F. C. Lee. "Modeling and applications of symmetry and balance techniques in reducing common mode EMI of PFCconverters". in Proc. 2008 CPES Power Electronics Seminar, pp. 128-135K. Elissa, "Title of paper if known," unpublished.

[3] S. Wang, Y. Y. Maillet, F. Wang, R. Lai, F. Luo, and D. Boroyevich, "Parasitic effects of grounding paths on common mode EMI filter's performance in power electronics systems," IEEE Transactions on Industrial Electronics., vol. 57, no. 9, pp. 3050–3059, Sep. 2010

[4] P. Kong , S. Wang , F. C. Lee and C. Wang "Common-mode EMI study and reduction technique for the interleaved multichannel PFC converter", IEEE Transactions on Power Electronics, vol. 23, no. 5, pp.2576 -2584, Sep. 2008

[5] D. Fu, S. Wang , P. Kong, F.C. Lee and D. Huang "Novel Techniques to Suppress the Common-Mode EMI Noise Caused by Transformer Parasitic Capacitances in DC–DC Converters", IEEE Transactions on Power Electronics, vol. 60, no. 11, pp.4968 -4977, Nov. 2013

[6] P. Kong , S. Wang and F. C. Lee "Common mode EMI noise suppression for bridgeless PFC converters", IEEE Transactions on Power Electronics, vol. 23, no. 1, pp.291 -297, Jan. 2008

[7] Cochrane, D.; Chen, D.Y.; Boroyevic, D., "Passive cancellation of common-mode noise in power electronic circuits,", IEEE Transactions on Power Electronics , vol.18, no.3, pp.756,763, May. 2003

[8] S. Lin, M. Zhou, W. Chen and J. Ying, "Novel methods to reduce common-mode noise based on noise balance," in Proc. 2006 IEEE Power Electronics Specialist Conf., pp. 2728 – 2733

[9] L. Xie, X. Ruan, Q. Ji, and Z. Ye "Shielding-cancellation technique for suppressing common mode EMI in isolated power converters", IEEE Transactions on Power Electronics, vol. 62, no. 5, pp.62(5), 2814-2822, May. 2015

[10] Y. Yang, D. Huang, F. C. Lee, and Q. Li, "Transformer shielding technique for common mode noise reduction in isolated converters," in Energy Conversion Congress and Exposition (ECCE), 2013 IEEE, pp. 4149-4153.